REMARKS

INTRODUCTION:

In accordance with the foregoing, claim 18 has been amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 4-6, 14, and 16-21 are pending and under consideration. Reconsideration is respectfully requested.

ENTRY OF RESPONSE UNDER 37 C.F.R. §1.116:

Applicant requests entry of this Rule 116 Response and Request for Reconsideration because:

(a) it is believed that the amendment of claim 18 puts this application into condition for allowance;

(b) the amendment was not earlier presented because the Applicant believed in good faith that the cited prior art did not disclose the present invention as previously claimed;

(c) the amendment of claim 18 should not entail any further search by the Examiner since no new features are being added or no new issues are being raised;

(d) the amendment does not significantly alter the scope of the claims and places the application at least into a better form for appeal. No new features or new issues are being raised.

The Manual of Patent Examining Procedures sets forth in §714.12 that "[a]ny amendment that would place the case either in condition for allowance or in better form for appeal may be entered." (Underlining added for emphasis) Moreover, §714.13 sets forth that "[t]he Proposed Amendment should be given sufficient consideration to determine whether the claims are in condition for allowance and/or whether the issues on appeal are simplified." The Manual of Patent Examining Procedures further articulates that the reason for any non-entry should be explained expressly in the Advisory Action.

REJECTION UNDER 35 U.S.C. §102:

In the Office Action, at pages 2-3, numbered paragraph 1, claims 18-21 were rejected under 35 U.S.C. §102(e) as being anticipated by Lauder et al. (USPN 6,130,823; hereafter, Lauder). This rejection is traversed and reconsideration is requested.

Claim 18 has been amended to recite: "A semiconductor device, comprising: a substrate having a main surface; a plurality of device layers stacked in succession on the main surface of the substrate, wherein each of the plural device layers comprises: a set of conductors comprising a wiring pattern, and an insulating layer formed on and embedding the set of conductors and having vias extending therethrough, and embedding therein a semiconductor element, and wherein a wiring pattern of a first device layer is electrically connected to a first semiconductor element embedded in a first insulating layer with a first set of conductors and one or more of a second set of conductors is/are electrically connected to the first semiconductor element embedded in a second insulating layer and through corresponding said vias to one or more of the first set of conductors," which is not taught or suggested by the stackable ball grid array of Lauder. The present claimed invention does not include a plurality of conductive balls affixed to the bottom surface of a support member, a plurality of conductive interconnect pads affixed to the top surface of the support member and a plurality of conductive vias through the support member, each of the conductive vias electrically connecting one of the balls to one of the interconnect pads and one or more electronic devices attached to the support member so that a chip select decoder electrically connected to the vias increases an address capacity of the vias, which is taught by Lauder.

Thus, it is respectfully submitted that it is clear that the integrated structure of the present claimed invention is different from the *modular* stack assemblage of stackable ball grid arrays of Lauder.

Hence, it is respectfully submitted that amended claim 18 is not anticipated under 35 U.S.C. §102(e) by Lauder et al. (USPN 6,130,823). Since claims 19-21 depend from amended claim 18, claims 19-21 are submitted not to be anticipated under 35 U.S.C. §102(e) by Lauder et al. (USPN 6,130,823) for at least the reasons that amended claim 18 is submitted not to be anticipated under 35 U.S.C. §102(e) by Lauder et al. (USPN 6,130,823).

REJECTION UNDER 35 U.S.C. §103:

In the Office Action, at pages 4-5, numbered paragraph 2, claims 4-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lauder et al. (USPN 6,130,823; hereafter, Lauder) in view of Itabashi et al. (USN 6,300,244; hereafter, Itabashi). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

It is respectfully submitted that amended claim 18 is not taught or suggested by Lauder since Lauder teaches a *modular* stack assemblage of stackable ball grid arrays, in contrast to

the present invention which recites an integrated structure. Thus, amended claim 18 is submitted to be patentable under 35 U.S.C. §103(a) over Lauder et al. (USPN 6,130,823). Since claims 4-6 depend from amended claim 18, claims 4-6 are submitted to be patentable under 35 U.S.C. §103(a) over Lauder et al. (USPN 6,130,823) for at least the reasons that amended claim 18 is submitted to be patentable under 35 U.S.C. §103(a) over Lauder et al. (USPN 6,130,823).

It is respectfully submitted that Itabashi teaches forming a wiring conductor on a semiconductor substrate, a via hole or a trench by directly performing electroless plating on a barrier layer containing a very small depressed portion such as a via-hole or the trench in an insulator layer without using a dry metallized method or a substitutive plating method. However, Itabashi fails to teach or suggest a semiconductor device, comprising: a substrate having a main surface; a plurality of device layers stacked in succession on the main surface of the substrate, wherein each of the plural device layers comprises: a set of conductors comprising a wiring pattern, and an insulating layer formed on and embedding the set of conductors and having vias extending therethrough, and embedding therein a semiconductor element, and wherein a wiring pattern of a first device layer is electrically connected to a first semiconductor element embedded in a first insulating layer with a first set of conductors and one or more of a second set of conductors is/are electrically connected to the first semiconductor element embedded in a second insulating layer and through corresponding said vias to one or more of the first set of conductors, as is recited by amended claim 18 of the present invention.

Thus, amended claim 18 is submitted to be patentable under 35 U.S.C. §103(a) over Itabashi et al. (USN 6,300,244). Since claims 4-6 depend from amended claim 18, claims 4-6 are submitted to be patentable under 35 U.S.C. §103(a) over Itabashi et al. (USN 6,300,244) for at least the reasons that amended claim 18 is submitted to be patentable under 35 U.S.C. §103(a) over Itabashi et al. (USN 6,300,244).

There is no teaching or suggestion of combining Lauder and Itabashi. The Examiner simply asserts that such a combination would have been obvious. Applicant submits that an argument can always be made that combining references would enhance or improve a certain feature because the claimed invention typically produces a benefit or improvement. Generally, the purpose in combining references is not to show that the combination will worsen or degrade a feature. However, the Examiner "can satisfy the burden of obviousness in light of combination 'only by showing some objective teaching [leading to the combination].'" In re Dembiczak, 50 USPQ2d 1614, 1617 (CAFC 1999), *quoting* In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992).

Further, "evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved ... The range of sources available, however, does not diminish the requirement for actual evidence." Dembiczak, 50 USPQ2d 1617. The Examiner has not provided evidence that the teaching he proposes actually exists in the prior art.

Thus, it is respectfully submitted that there is no teaching or suggestion of combining Lauder et al. (USPN 6,130,823) in view of Itabashi et al. (USN 6,300,244), and even if combined, Lauder et al. (USPN 6,130,823) and Itabashi et al. (USN 6,300,244) do not teach or suggest amended claim 18 of the present invention. Thus, amended claim 18 is submitted to be patentable under 35 U.S.C. §103(a) over Lauder et al. (USPN 6,130,823) in view of Itabashi et al. (USN 6,300,244). Since claims 4-6 depend from amended claim 18, claims 4-6 are submitted to be patentable under 35 U.S.C. §103(a) over Lauder et al. (USPN 6,130,823) in view of Itabashi et al. (USN 6,300,244) for at least the reasons that amended claim 18 is submitted to be patentable over Lauder et al. (USPN 6,130,823) in view of Itabashi et al. (USN 6,300,244).

ALLOWED CLAIMS:

Claims 14, 16, and 17 are allowed.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited. At a minimum, this Amendment should be entered at least for purposes of Appeal as it either clarifies and/or narrows the issues for consideration by the Board.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited and possibly concluded by the Examiner contacting the undersigned attorney for a telephone interview to discuss any such remaining issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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